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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/748,551	12/30/2003	Joseph B. Rowlands	BP1735CON	8455

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EXAMINER	
LI, ZHUO H	

ART UNIT	PAPER NUMBER
2185	

DATE MAILED: 10/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary	Application No.	Applicant(s)	
	10/748,551	ROWLANDS ET AL.	
	Examiner	Art Unit	
	Zhuo H. Li	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *19-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *19-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12/30/03* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/26/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement filed on July 26, 2004 fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each cited foreign patent document; each non-patent literature publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed. It has been placed in the application file, but the information referred to therein has not been considered.

Response to Amendment

2. This Office action is in respond to the Preliminary amendment filed on 7/26/2004. Claims 1-18 are canceled, and claims 19-36 are pending in the application for examination.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 19-27are rejected under 35 U.S.C. 102(e) as being anticipated by Cho (US PAT. 6,240,532).

Regarding claim 19, Cho discloses a method to test a cache via the testing logic (42, figure 4) in the cache system (40, figure 4) comprising performing a direct access transaction of a cache to directly select a cache entry, i.e., address (54, figure 4) for a transaction (col. 4 lines 49-52 and col. 5 lines 33-41), the direct access transaction overriding a hit or miss protocol, i.e., by the forced hit signal (col. 6 lines 33-43), used with the cache when memory transactions are to be performed (col. 5 lines 42-61), and performing test by using the selected entry access by the direct access transaction (col. 5 line 62 through col. 6 line 15 and figure 5)

Regarding claim 20, Cho discloses the method of performing the direct access transaction includes selecting a particular way, i.e., four-way associative cache (col. 2 lines 28-40) for a next eviction, i.e., with a force hit signal, data is written in and read out from the data RAM (figure 4) in X and/or Y array regardless the errors in the tag RAM portion (steps 80-85, figure 5 and col. 5 lines 42-61), and the performing the test includes performing a selected memory transaction, i.e., read transaction, which results in a cache miss evicting an entry of the selected way, i.e., a read transaction from Tag RAM is perform to test whether the data written in the data RAM is corrected or not (col. 5 lines 62-67 and steps 86-88, figure 5), if an error occur, the corrected data is replaced by load updated data from system memory into the corresponding data entry with replacement algorithm (col. 6 lines 1-15 and steps 90-92, figure 5).

Regarding claims 21 and 23, Cho discloses the method comprising performing a read memory transaction, in which data from memory is cached into the entry of the selected way, and performing the test transaction includes performing a write memory transaction, in which data to be stored in memory is cached into the entry of the selected way (col. 5 lines 42-67, figure 5 and col. 6 lines 43-48).

Regarding claims 22 and 24, Cho discloses the method further comprising performing a second direct access transaction, i.e., read transaction from the tag RAM cache to compare whether the data stored is correct or not via the comparators (56 and 58, figure 4 and steps 86-92, figure 5), to access the entry of the selected way and comparing the cached data to the data in the memory or the data originally selected to be written (col. 5 line 62 through col. 6 line 15 and col. 6 lines 53-59).

Regarding claim 25, Cho discloses the method of performing the test transaction includes performing a memory transaction of test data, i.e., read transaction, that results in a miss in the cache and in which the miss causes an eviction, i.e., replacement, and caches the test data into the entry of the selected way, i.e., L set location, (col. 5 line 42 through col. 6 line 15 and figure 5).

Regarding claim 26, Cho discloses the method further comprising performing a second direct access transaction, i.e., read transaction from the tag RAM cache to compare whether the data stored is correct or not via the comparators (56 and 58, figure 4 and steps 86-92, figure 5), to access the entry of the selected way and comparing the cached data to the test data for error (col. 5 line 42 through col. 6 line 15 and col. 6 lines 53-59).

Regarding claim 27, Cho discloses the method further comprising reading a tag of the selected entry with a tag stored in a tag register, i.e., tag RAM cache (figure 4), to compare the two tags for error via the comparators (56 and 58, figure 4 and col. 5 line 42 through col. 6 line 15).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 28-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cho (US PAT. 6,240,532) in view of Vanka et al. (US PAT. 5,479,636 hereinafter Vanka).

Regarding claim 28, Cho discloses a method to reset a cache comprising performing a direct access transaction of a cache (40, figure 4) to directly select a cache entry (54, figure 4) for the transaction, the direct access transaction overriding a hit or miss protocol used with the cache, i.e., via the force hit signal (col. 6 lines 33-43), when memory transactions are to be performed (col. 5 lines 42-61). Cho differs from the claimed invention in not specifically teaches the direct access transaction setting an indication that the selected entry is invalid, and performing a memory transaction to generate a cache miss and to have a predetermine data written into the selected entry by eviction of invalid data to store predetermined data as reset data

for the selected entry. However, Vanka teaches the computer system (figure 1) comprising a CPU (10, figure 1) initial a memory transaction to cache memory (30, figure 1) via the cache and memory controller (20, figure 1), and when the memory transaction is missed, i.e., invalid entry in the cache, the cache and memory controller simultaneously initiates a writing operation to write the invalid entry out to the write buffer (50, figure 1), i.e., eviction of invalid data, and a reading operation to load the updated entry from the lower level memory into the cache and CPU (col. 6 line 28 through col. 7 line 16), i.e., store predetermined data as reset data for the selected entry. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the computer system of Cho in having a steps of setting an indication that the selected entry is invalid, and performing a memory transaction to generate a cache miss and to have a predetermine data written into the selected entry by eviction of invalid data to store predetermined data as reset data for the selected entry, as per teaching by the computer system of Vanka, because it minimizing the stalling of the CPU (col. 8 lines 52-56), prevents improperly overwrite portions of the old line in cache before the old line could be saved (col. 7 lines 36-37), and provides the maximum extend possible which valuable processor cycles are not wasted waiting for the new cache line (col. 8 lines 14-17).

Regarding claim 29, Cho discloses a method wherein the performing the direct access transaction includes selecting a selected index, i.e., tag entry in Tag RAM cache, and way, i.e., L way, of a cache line for eviction, i.e., replacement (col. 5 line 62 through col. 6 line 15).

Regarding claim 30, Cho discloses the method wherein the performing the direct access and the performing the memory transaction are repeated for entries of the cache to stored respective predetermined data in the cache to reset the cache to a known state, i.e., when the

force hit signal is turned off, a read transaction is performed to read the Tag RAM to determent the data previously stored is correct or not when the force hit signal was on (col. 5 lines 62-67), and if incurred is occurred, replacement is performed (col. 6 lines 1-15 and lines 52-59).

Regarding claim 31, Cho discloses the method to synchronize a cache comprising performing a direct access transaction of a cache (40, figure 4) to directly select a cache way, the direct access transaction used to override a hit or miss protocol used with the cache, i.e., via the force hit signal (col. 5 lines 42-60 and col. 6 lines 34-43) when memory transactions are to be performed. Cho differs from the claimed invention in not specifically teaches the direct access transaction comprising initialize a replacement procedure that is used for cache misses, and performing subsequent memory transactions, in which way replacement is synchronized to commence from a known initialized way. However, Vanka teaches the computer system (figure 1) comprising a CPU (10, figure 1) initial a memory transaction to cache memory (30, figure 1) via the cache and memory controller (20, figure 1), and when the memory transaction is missed, i.e., invalid entry in the cache, the cache and memory controller simultaneously initiates a writing operation to write the invalid entry out to the write buffer (50, figure 1), i.e., eviction of invalid data, and a reading operation to load the updated entry from the lower level memory into the cache and CPU, i.e., way replacement operation (col. 6 line 28 through col. 7 line 16), in addition, Vanka teaches an subsequent access is able to generate by the CPU after the replacement operation is completed, and the updated entry is written into the cache memory (col. 8 line 57 through col. 9 line 2). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the computer system of Cho in having steps of comprising initialize a replacement procedure that is used for cache misses, and

performing subsequent memory transactions, in which way replacement is synchronized to commence from a known initialized way, as per teaching by the computer system of Vanka, because it minimizing the stalling of the CPU (col. 8 lines 52-56), prevents improperly overwrite portions of the old line in cache before the old line could be saved (col. 7 lines 36-37), and provides the maximum extend possible which valuable processor cycles are not wasted waiting for the new cache line (col. 8 lines 14-17).

Regarding claim 32, Cho discloses the method further comprising writing test data into cache starting from the known initialized way, i.e., directly write data into the data RAM cache with force hit signal (col. 5 lines 30-61 and figure 5).

Regarding claim 33, the limitations of the claim are rejected as the same reasons set forth in claim 28.

Regarding claim 34, Cho discloses the method wherein the performing the direct access transaction selects an index, i.e., tag and way of the cache and the performing the memory transaction flushes a cache line identified by the memory transaction to memory, i.e., incorrect/dirty data write back to the main memory (col. 6 lines 1-6 and lines 49-59).

Regarding claims 35-36, Cho discloses the method wherein the cache entry is set for eviction by setting the entry as invalid, i.e., via the validity bit and/or dirty bit in the tag RAM cache in the Tag RAM miss test (figure 5), the cache entry is set for flushing by setting the entry as dirty, i.e., incorrect/dirty data write back to the main memory (col. 5 line 30 through col. 6 line 59).

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Auvinen et al. (US PAT. 5,276,833) discloses data cache management system with test mode using index registers and CAS disable and posted write disable (col. 1 line 61 through col. 2 line 35).

Keeley (US PAT. 4,575,792) discloses shared interface apparatus for testing the memory sections of a cache unit (Abstract).

Finch et al. (US PAT. 5,524,208) discloses method and apparatus for performing cache snoop testing using DMA cycles in a computer system (col. 4 line 23 through col. 6 line 10).

Oura (US PAT. 6,701,461) discloses method and apparatus for testing a cache wherein a plurality of testing commands can be created in which memory access address are set randomly and the block to be accessed are set without duplication (col. 1 line 63 through col. 4 line 34).

Lin (US PAT. 5,423,019) discloses automatic cache flush with readable and writable cache tag memory (Abstract).

Fuccio et al. (US PAT 5,249,281) discloses Testable RAM architecture in a microprocessor having embedded cache memory (Abstract).

Cooper (US PAT. 5,671,231) discloses method and apparatus for performing cache snoop testing on a cache system (col. 4 lines 10-54).

Suzuki (US PAT. 5,274,790) discloses cache memory apparatus having plurality of accessibility ports which comprising a replacement control circuit operates for replacing data and corresponding tag information in the cache memory when the cache-missing is discriminated by the hit discriminating circuit (25-26,f figure 2, and col. 2 line 18 through col. 3 line 7).

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zhuo H. Li whose telephone number is 571-272-4183. The examiner can normally be reached on M-F 9:00am - 6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

10. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Zhuo H. Li

Patent Examiner
Art Unit 2189
September 1, 2005

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